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## \*BIBDATASHEET\*

**CONFIRMATION NO. 5415** 

ib Data Sheet									
SERIAL NUMBER 02/26/2002 10/082,055		CLASS 702		GROUP ART UNIT 2857		ATTORNEY DOCKET NO. 100021-00072			
	RULE								
PPLICANTS									
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* CONTINUING DATA *	**************************************								
FOREIGN APPLICATION 14PAN 2001-269	ONS *********								
IF REQUIRED, FOREIG	N FILING LICENSE GRAN	TED							
** 03/20/2002 Foreign Priority claimed yes no STATE OR					ETS	т	OTAL	INDEPENDENT	
35 USC 119 (a-d) conditions	COUNTRY JAPAN	DRA	DRAWING 0		LAIMS 44	CLAIMS 4			
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20036-5339									
TITLE			in a nut vorifica	ation of conf	ection of	nodes			
Test circuit and semicor	nductor integrated circuit eff	ectively carry	/ing out vernica	audit di daim	☐ All Fe				
	EES: Authority has been given in Paper o to charge/credit DEPOSIT ACCOUNT o for following:				1.16 Fees ( Filing )				
					1.17 Fees ( Processing Ext. of time )				
					1.18 Fees ( Issue )				
RECEIVED No					Other				
1256						☐ Credit			